COM422/AT

Single or Dual Channel RS-422 Communications Adapter

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COM422/AT
User's Manual

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COM422/AT User's Manual

1.1 Introduction

The COM422/AT is a dual channel RS-422 asynchronous serial communications adapter for systems implementing a 16-bit ISA compatible I/O bus. The COM485/AT is an RS-485 version of this adapter. Data is communicated through two shielded D-9 connectors which provide greater shielding from environmental noise.

The serial interface is implemented with a pair of 16450 Asynchronous Communication Elements (ACEs). The 16450 is compatible with the 8250 ACE found in the original IBM PC/XT models. The optional 16550 ACE provides an additional FIFO mode of operation which reduces CPU overhead at higher data rates.

The COM422/AT and COM485/AT allow independent addressing of each channel through a set of address decode switches (SW1 through SW4). These switches allow each channel to be addressed anywhere in the available I/O address space of the system. Each channel is also capable of selecting and/or sharing one of eleven possible interrupt request (IRQ) lines: IRQ 2-7, 10-12, 14-15.

NOTE

The optional 16550 ACE has been installed within your IOtech COM422/AT board.

1.2 Board Description

The first channel of the COM422/AT is controlled by the ACE labeled U9, switches SW1 & SW2 for addressing, jumper J10 for interrupts, and jumper J2 for signal assignment. Channel 1 is accessed through the RJ-11 connector labeled CON1.

The remaining seven channels and their corresponding signal-assignment jumpers are as follows: Channel 2 is labeled U14 with jumper J3, Channel 3 is labeled U10 with jumper J4, Channel 4 is labeled U15 with jumper J5, Channel 5 is labeled U11 with jumper J6, Channel 6 is labeled U16 with jumper J7, Channel 7 is labeled U12 with jumper J8, and Channel 8 is labeled U17 with jumper J9. The address of each of the ports are incremented by a factor of 8 in hexadecimal code. In other words, if Channel 1 was at a address of 0300H, Channel 2 would be at 0308H. The input clock frequency is controlled by jumper J1.

1.3 Specifications

Bus interface: ISA 16-bit bus

Controllers: 2 - 16450 Asynchronous Communication Elements (ACEs)

(Optional 16550 ACEs)

Interface: 2 - D-9 female connectors

Transmit drivers:
MC3487 or compatible (RS-422)
TI75174 or compatible (RS-485)

Receive buffers:
MC3486 or compatible (RS-422)
TI75175 or compatible (RS-485)

I/O Address range: 0000H - FFFFH

Interrupt levels: IRQ 2, 3, 4, 5, 6, 7, 10, 11, 12, 14, 15

Power requirements:

I_T	IMS	Supply
497mA	564mA	+5 Volts
—	—	+12 Volts
—	—	-12 Volts

I_T - Typical adapter current

I_{MS} - Maximum statistical adapter current

1.4 16450/16550 Functional Description

The 16450 is an improved specification version of the industry standard 8250 Asynchronous Communications Element (ACE) and is a functionally equivalent replacement. This ACE performs serial-to-parallel conversion on data characters received and parallel-to-serial conversion on data output from the CPU.

Designed to be compatible with the 16450, the 16550 ACE enters character mode on reset and in this mode appears as a 16450 to user software. An additional mode, FIFO mode, can be invoked to reduce CPU overhead. The FIFO mode increases performance by providing two 16-byte FIFOs (one transmit and one receive) to buffer data and reduce the number of interrupts issued to the CPU.

Other features of the 16450/16550 include:

- Programmable baud rate, character length, parity, and number of stop bits.
- Automatic addition and removal of start, stop, and parity bits.
- Independent and prioritized transmit, receive and status interrupts.

The following pages provide a brief summary of the internal registers available within the 16450 and 16550 ACEs. The registers are addressed as shown in the table below. Registers specific to the 16550 will be marked with an asterisk(*). NOTE: DLAB is accessed through the Line Control Register.

DLAB	A2	A1	A0	Register Description
0	0	0	0	Receive buffer (read only) Transmitter holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only) FIFO control* (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

Figure 1: Internal Register Map for 16450 & 16550 ACEs

1.4.1 Interrupt Enable Register

The bit definitions for this register are as follows:

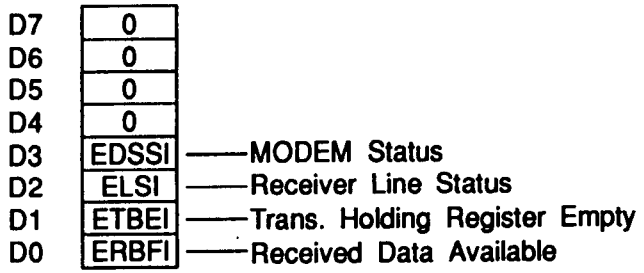


Figure 2: Interrupt Enable Register Definitions

EDSSI MODEM Status Interrupt:	When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.
ELSI Receiver Line Status Interrupt:	When set (logic 1), enables interrupt on overrun, parity, framing errors, and break indication.
ETBEI Transmitter Holding Register Empty Interrupt:	When set (logic 1), enables interrupt on transmitter register empty.
ERBFI Received Data Available Interrupt:	When set (logic 1), enables interrupt on received data available or FIFO trigger level.

* For Optional 16550 only.

1.4.2 Interrupt Identification Register

The bit definitions for this register as as follows:

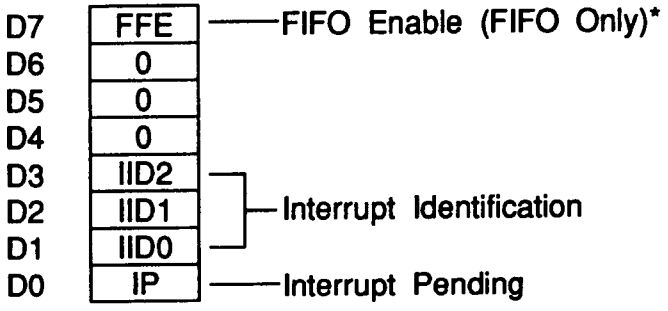


Figure 3: Interrupt Identification Register Definitions

FFE FIFO Enable:*	When logic 1, indicates FIFO mode enabled.
IIDx Interrupt Identification:	Indicates highest priority interrupt pending if any. See IP and Figure 4. NOTE: IID2 is always a logic 0 in the 16450 and in character mode.
IP Interrupt Pending:	When logic 0, indicates that an interrupt is pending and the contents of the interrupt identification register may be used to determine the interrupt source. See IIDx and Figure 4.

* For Optional 16550 only.

IID2	IID1	IID0	IP	Priority	Interrupt Type
x	x	x	1	N/A	None
0	1	1	0	Highest	Receiver Line Status
0	1	0	0	Second	Received Data Ready
1	1	0	0	Second	Character Timeout* (FIFO only)
0	0	1	0	Third	Transmitter Holding Register Empty
0	0	0	0	Fourth	MODEM Status

Figure 4: Interrupt Identification Bit Definitions

Receiver Line Status:	Indicates overrun, parity, framing errors or break interrupts. The interrupt is cleared by reading the line status register.
Received Data Ready:	Indicates receiver data available. The interrupt is cleared by reading the receiver buffer register.
FIFO mode:*	Indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the trigger level.
Character Timeout:* (FIFO mode only)	Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is at least one character in the FIFO during this time. The interrupt is cleared by reading the receiver FIFO.
Transmitter Holding Register Empty:	Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register.
MODEM Status:	Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

* For Optional 16550 only.

1.4.3 FIFO Control Register

For Optional 16550 Only

The bit definitions of this register are as follows:

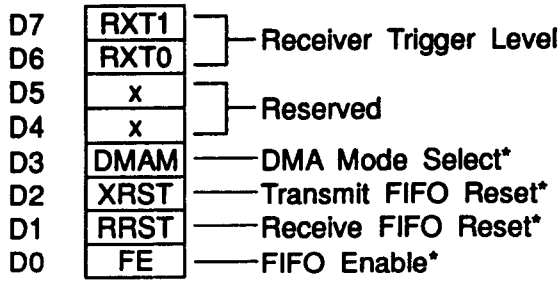


Figure 5: FIFO Control Register

RXTx - Receiver FIFO Trigger Level:*	Determines the trigger level for given in the table below.

RXT1	RXT0	Trigger Level (bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Figure 6: FIFO Trigger Levels

DMAM DMA Mode Select:*	When set (logic 1), RxRDY and mode 0 to mode 1. DMA mod COM422/AT and COM485/AT.
XRST Transmit FIFO Reset:*	When set (logic 1), all bytes in are cleared and the counter is r is not cleared. XRST is self-cle

1.4.3 FIFO Control Register

For Optional 16550 Only

The bit definitions of this register are as follows:

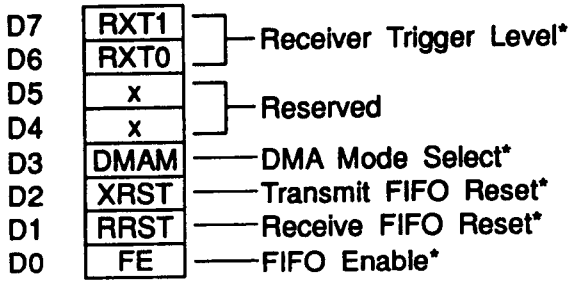


Figure 5: FIFO Control Register

RXTx - Receiver FIFO Trigger Level:*	Determines the trigger level for the FIFO interrupt as given in the table below.

RXT1	RXT0	Trigger Level (bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Figure 6: FIFO Trigger Levels

DMAM DMA Mode Select:*	When set (logic 1), RxRDY and TxRDY change from mode 0 to mode 1. DMA mode is not supported on COM422/AT and COM485/AT.
XRST Transmit FIFO Reset:*	When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.

RRST Receive FIFO Reset:*	When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.
FE FIFO Enable:*	When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.

* For Optional 16550 only.

1.4.4 Line Control Register

The bit definitions for this register are as follows:

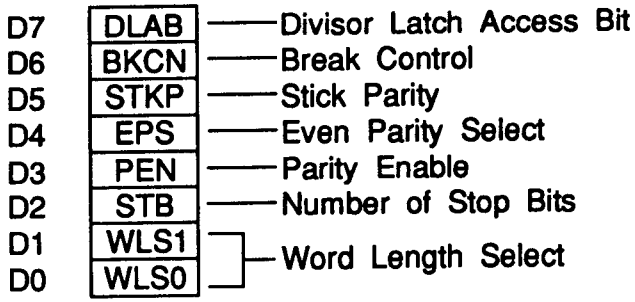


Figure 7: Line Control Register

DLAB Divisor Latch Access Bit:	DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.
BKCN Break Control:	When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).
STKP Stick Parity:	Forces parity to logic 1 or logic 0 if parity is enabled. See EPS, PEN, and Figure 8.
EPS Even Parity Select:	Selects even or odd parity if parity is enabled. See STKP, PEN, and Figure 8.
PEN Parity Enable:	Enables parity on transmission and verification on reception. See EPS, STPK, and Figure 8.

STKP	EPS	PEN	Parity
x	x	0	None
0	0	1	Odd
0	1	1	Even
1	0	1	Logic 1
1	1	1	Logic 20

Figure 8: 16450/16550 Parity Selections

STB Number of Stop Bits:	Sets the number of stop bits transmitted. See WLSx and Figure 9.
WLSx Word Length Select:	Determines the number of bits per transmitted word. See STB and Figure 9.

STB	WLS1	WLS0	Word Length	Stop Bits
0	0	0	5 bits	1
0	0	1	6 bits	1
0	1	0	7 bits	1
0	1	1	8 bits	1
1	0	0	5 bits	1 1/2
1	0	1	6 bits	2
1	1	0	7 bits	2
1	1	1	8 bits	2

Figure 9: Word Length and Stop Bit Selections

1.4.5 Modem Control Register

The bit definitions for this register are as follows:

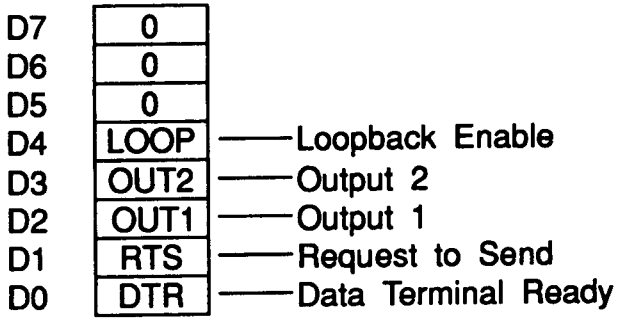


Figure 10: MODEM Control Register Definitions

LOOP Loopback Enable:	When set (logic 1), the transmitter shift register is internally connected to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state. Transmit and receive interrupts operate normally but MODEM control interrupts are available but are now controlled through the MODEM control register.

Bits OUT2, OUT1, RTS, and DTR perform identical functions on their respective outputs. When these bits are set (logic 1) in the register, the associated output is forced to a logic 0. When cleared (logic 0), the output is forced to a logic 1.

OUT2 Output 2:	Controls the OUT2 output, as described above. Used for interrupt enable, see Section 1.8.
OUT1 Output 1:	Controls the OUT1 output, as described above. OUT1 is unused on the COM422/AT and the COM485/AT.
RTS Request To Send:	Controls the RTS output, as described above. Used for output driver control, see Section 1.9.
DTR Data Terminal Ready:	Controls the DTR output, as described above. Used for output driver control, see Section 1.9.

1.4.6 Line Status Register

The bit definitions for this register are as follows:

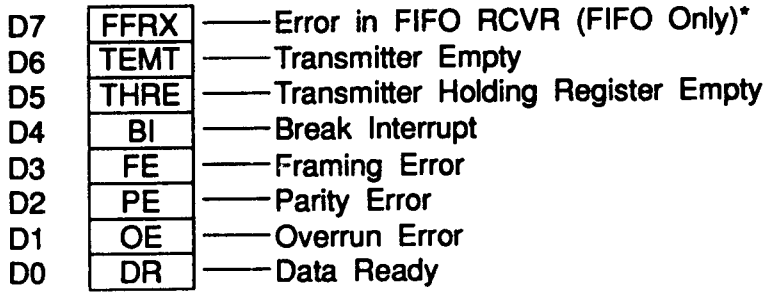


Figure 11: Line Status Register Definitions

FFRX FIFO Receiver Error:*	Logic 0 in 16450 and 16550 character mode.
FIFO mode:	Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.
TEMT Transmitter Empty:	Indicates the transmitter holding register (or FIFO*) and the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.
THRE Transmitter Holding Register Empty:	Indicates the transmitter holding register (or FIFO*) is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register (or FIFO).

* For Optional 16550 only.

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. In FIFO mode*, these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

BI Break Interrupt:	Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time.
FIFO mode:*	Only one zero character is loaded into the FIFO and transfers are disabled until SIN goes to the mark state (logic 1) and a valid start bit is received.
FE Framing Error:	Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).
PE Parity Error:	Indicates that the received data does not have the correct parity.
OE Overrun Error:	Indicates the receive buffer was not read before the next character was received and the character is destroyed.
* FIFO mode:	Indicates the FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.
DR Data ready:	Indicates data is present in the receive buffer (or FIFO). DR is reset by reading the receive buffer register.

* For Optional 16550 only.

1.4.7 Modem Status Register

The bit definitions for this register are as follows:

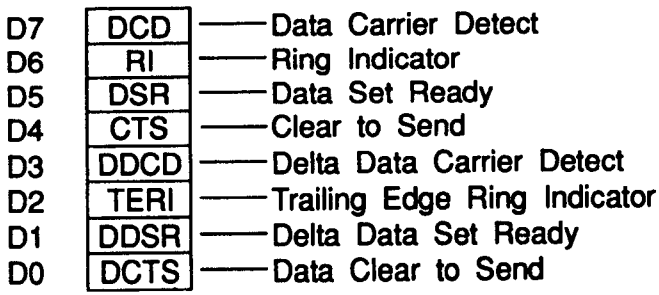


Figure 12: MODEM Status Register Definitions

DCD Data Carrier Detect:	Complement of the DCD input.
RI Ring Indicator:	Complement of the RI input.
DSR Data Set Ready:	Complement of the DSR input.
CTS Clear To Send:	Complement of the CTS input.

Bits DDCD, TERI, DDSR, and DCTS are the sources of MODEM status interrupts. These bits are reset when the MODEM status register is read.

DDCD Delta Data Carrier Detect:	Indicates the Data Carrier Detect input has changed state.
TERI Trailing Edge Ring Indicator:	Indicates the Ring Indicator input has changed from a low to a high state.
DDSR Delta Data Set Ready:	Indicates the Data Set Ready input has changed state.
+DCTS Delta Clear To Send:	Indicates the Clear to Send input has changed state.

1.4.8 Scratchpad Register

This register is not used by the 16450 or 16550 ACEs. It may be used by the programmer for data storage.

1.5 FIFO Interrupt Mode Operation

For Optional 16550 Only

1. The receive data interrupt is issued when the FIFO reaches the trigger level. The interrupt is cleared as soon as the FIFO falls below the trigger level.
2. The interrupt identification register's receive data available indicator is set and cleared along with the receive data interrupt above.
3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.

1.6 Baud Rate Selection

The 16450 and 16550 ACEs determine the baud rate of the serial output using a combination of the input clock frequency and the values contained in the divisor latches. Standard PC, PC/XT, PC/AT, and PS/2 serial interfaces use an input clock of 1.8432 Mhz. To increase versatility, the COM422/AT uses an 18.432 Mhz crystal and a frequency divider circuit to produce the standard input clock frequency.

Jumper J1 is used to set the frequency input to the 16450/16550. It may be connected to divide the clock input by 1, 2, 5, or 10. For compatibility, J1 should be configured to divide by 10 as shown in Figure 13(d). A table of baud rates available using the 1.8432 Mhz input is given in Figure 14.

* For Optional 16550 only.

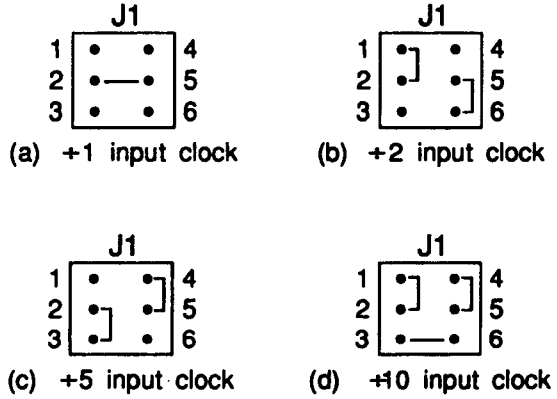


Figure 13: Input Clock Frequency Options

NOTE: For compatibility, the jumper should be set at +10 (18.432 Mhz +10 = 1.8432 Mhz).

The following table lists divisor latch settings for common baud rates using an 1.8432 Mhz input clock. For compatibility, connect jumper in the divide by 10 configuration (Figure 13(d)).

Desired Baud Rate	Divisor Latch Value	Error Between Desired and Actual Value (%)
50	2304	—
75	1536	—
110	1047	0.026
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Figure 14: Divisor Latch Settings

1.7 Addressing

Each channel of the COM422/AT or the COM485/AT uses eight consecutive I/O address locations in the range 0 to FFFF Hex. The base address of channel 1 is selected using dip switches SW1 and SW2 while the base address of channel 2 is selected using SW3 and SW4. The first 13 switch positions define address lines A15 through A3 respectively. A switch set to the "ON" position requires the corresponding address bit to be "0" for selection while a switch set to the "OFF" position requires the address bit to be "1". Some address selection examples are given in Figure 16.

The fourteenth switch of each set, SW2 position 6 and SW4 position 6, are used to enable or disable the corresponding communication channel. When this switch is set to the "ON' position, the channel is fully operational. Setting this switch to the "OFF" position disables the channel.

The switch 1 and 2 in the figure below shows an address selection of channel 1. The address is set for 03F8H. Switches 3 and 4 show the base address for channel 2 set for 02F8H.

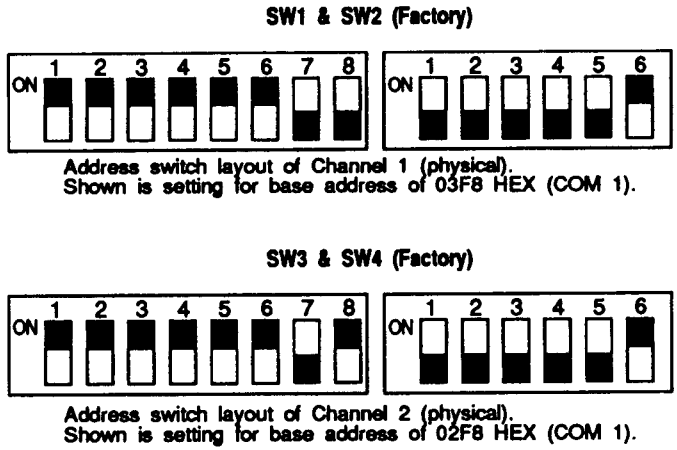


Figure 15: Factory Address Switch Settings

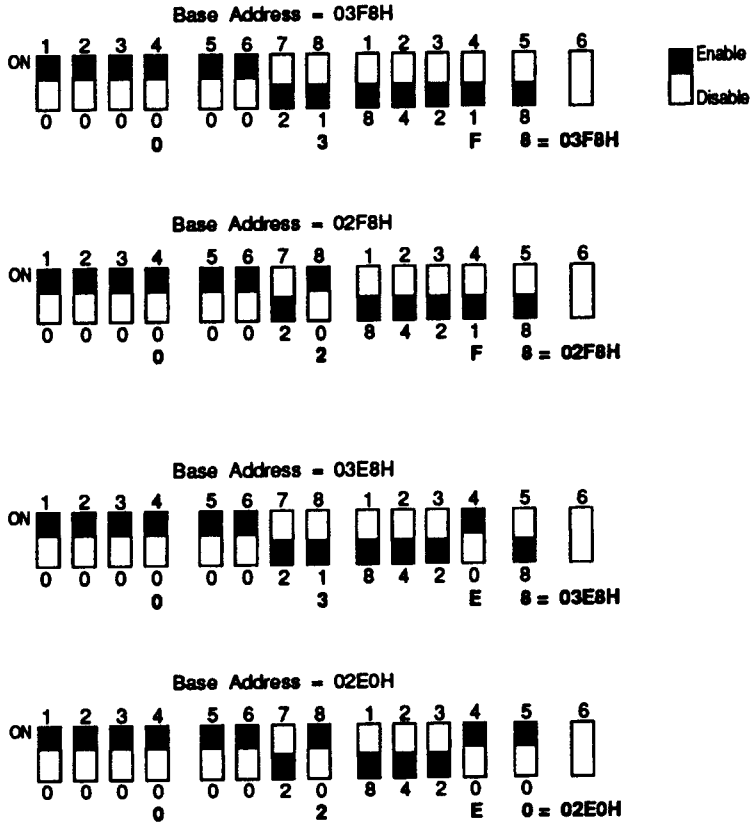


Figure 16: Address Switch Selection Examples

1.8 Interrupts

Each channel of the COM422/AT or the COM485/AT may select one of eleven possible interrupt request levels (IRQ 2-7, 10-12, 14-15). The interrupt request level is selected using jumper J3 for channel 1 and jumper J4 for channel 2 as shown in the figure below.

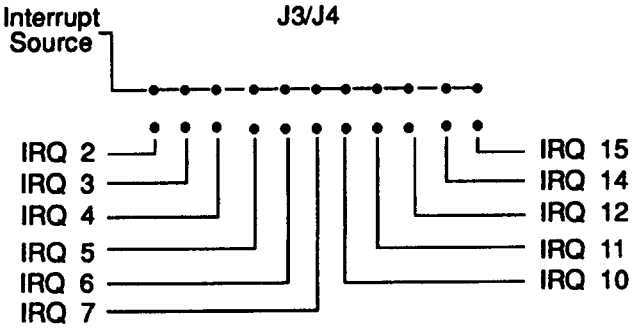
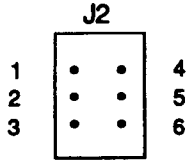


Figure 17: Interrupt Level Selection Jumper

An additional feature of the COM422/AT and the COM485/AT is the ability to share one interrupt level between both communication channels, or to share an interrupt level with another IOtech adapter supporting this interrupt sharing feature. Jumper J2 is used to control the interrupt sharing capability.



J2	Interrupt Operation	
Channel 1	1-2 2-3	Dedicated interrupt level Interrupt sharing enabled
Channel 2	4-5 5-6	Dedicated interrupt level Interrupt sharing enabled

NOTE: To be 100% ISA compatible, jumper 2 must be set to the dedicated interrupt level positions.

1.9 Output Configurations

Four sets of jumpers are implemented on the COM422/AT and the COM485/AT to control the auxiliary channel configuration and tri-state output drivers. Jumpers J5 and J6 and jumpers J7 and J8 perform the identical functions on channels 1 and 2 respectively. The figure below shows the output control block diagram.

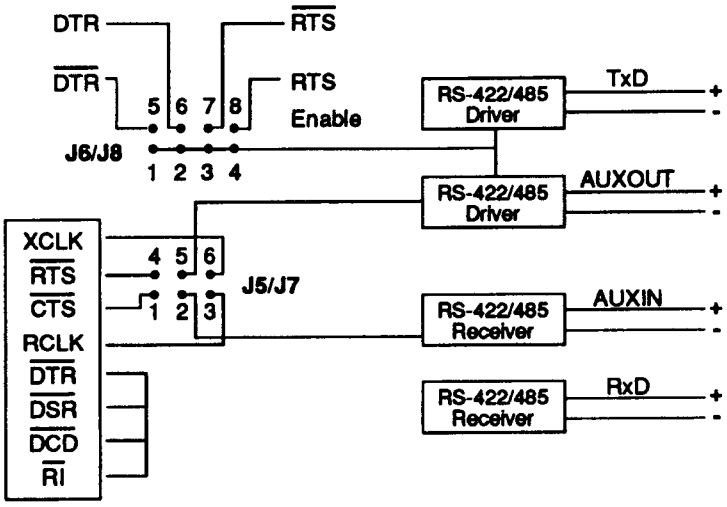


Figure 18: Output Control Block Diagram

1.9.1 Auxiliary Channel Configuration

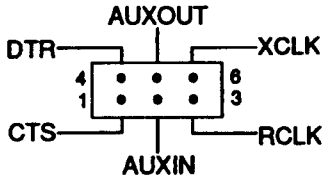
The function of jumpers J5 and J7 is to control the source of the information exchanged on the auxiliary communication lines. The output sources are request to send (RTS), transmit clock (XCLK), and the auxiliary input (AUXIN). The inputs selections are clear to send (CTS) and receive clock (RCLK).

Transmission of RTS, when combined with reception of CTS, allows for handshaking between the ACE and a peripheral device. RTS is transmitted by connecting pins 4 and 5 of the jumper block (figure 19a). CTS is received by connecting pins 1 and 2 (figure 19a). The RTS/CTS handshake can be defeated by looping the RTS output back to the CTS input. This is accomplished by connecting pins 1 and 4 (figures 19b and 19c).

RCLK is the input to the ACE that controls the shift rate of the receiver portion of the chip. Generally, this input is provided by connecting it to the transmit clock, XCLK, output from the ACE. This is accomplished by connecting pins 3 and 6 of the jumper (figures 19a and 19c). RCLK may be received from an external source by connecting pins 2 and 3 (figure 19b).

Transmission of XCLK can be used to synchronize communications with a peripheral or to provide a shift clock to a receiver. XCLK is transmitted by connecting pins 5 and 6 of the jumper block (figure 19b).

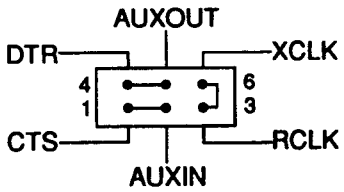
AUXIN is the auxiliary input from a peripheral device. Connecting AUXIN to AUXOUT provides a loopback mode of operation. That is, whatever is transmitted by the peripheral will be fed back to the peripheral. This is implemented by connecting pins 2 and 5 of the jumper block (figure 19c).



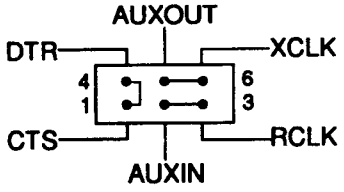
J5 = channel 1 J7 = channel 2

Function	J5/J7
RTS/CTS loopback*	1-4
Transmit RTS	4-5
Receive CTS	1-2
RCLK/XCLK loopback*	3-6
Transmit XCLK	5-6
Receive RCLK	2-3
AUXOUT/AUXIN loopback*	2-5

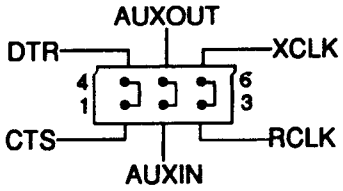
* - Indicates factory jumper settings.



(a) RTS transmission
CTS reception
XCLK/RCLK loopback



(b) RTS/CTS loopback
XCLK transmission
RCLK reception



(c) RTS/CTS loopback
XCLK/RCLK loopback
AUXOUT/AUXIN loopback

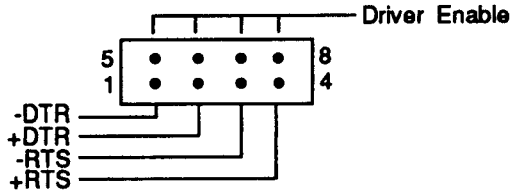
Figure 19: Auxiliary Channel Configuration

1.9.2 Half Duplex Operation

The function of jumpers J6 and J8 is to configure the communication channel for half or full duplex operation. Full duplex operation requires a connection between pins 5 and 6 of the jumper block. Half duplex operation requires one jumper connected vertically across jumper J6 for channel 1 or J8 for channel 2 (see figure 20 below). This connection allows the transmitter to be enabled and disabled using the data terminal ready (DTR) or request to send (RTS) outputs controlled through the modem control register of the 16450/16550.

CAUTION

When operating in half duplex mode, the transmitter must be disabled before receiving any information. Failure to do so will result in two output drivers being connectedtogether which may cause damage to the adapter, the computer, and/or the peripheral equipment.



Use J6 for channel 1, J8 for channel 2.

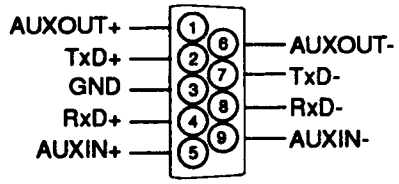
Figure 20: Half Duplex Control Jumper

If a jumper is installed between pins 2 and 6, the output drivers are controlled by the ACE's DTR signal. Setting DTR (logic 1) enables the drivers for both the data and auxiliary channel outputs while clearing DTR (logic 0) forces both outputs to a high impedance state. If the jumper is installed between pins 1 and 5 the logical sense of DTR is inverted. That is, clearing DTR (logic 0) enables the transmitter drivers while setting DTR (logic 1) forces the outputs to a high impedance state.

If a jumper is installed between pins 4 and 8, the output drivers are controlled by the ACE's RTS signal. Setting RTS (logic 1) enables the drivers for both the data and auxiliary channel outputs while clearing RTS (logic 0) forces both outputs to a high impedance state. If the jumper is installed between pins 3 and 7 the logical sense of RTS is inverted. That is, clearing RTS (logic 0) enables the transmitter drivers while setting RTS (logic 1) forces the outputs to a high impedance state.

1.10 External Connections

Connections to peripheral equipment are made via female D-9 connectors CN1 and CN2. A pin-out of the connectors and a description of each connector signal is given in the figure and table below.



D-9 Connector

Figure 21: Output Connector Pinouts

Pin	Signal	Description
1	AUXOUT+	When combined with AUXOUT-, provides the auxiliary channel output defined by jumper J8/J10.
2	TxD+	When combined with TxD-, provides the serial data output.
3	GND	Chassis ground.
4	RxD+	When combined with RxD-, provides the serial data input.
5	AUXIN+	When combined with AUXIN-, provides the auxiliary channel input defined by jumper J8/J10.
6	AUXOUT-	When combined with AUXOUT+, provides the auxiliary channel output defined by jumper J8/J10.
7	TxD-	When combined with TxD+, provides the serial data output.
8	RxD-	When combined with RxD+, provides the serial data input.
9	AUXIN-	When combined with AUXIN+, provides the auxiliary channel input defined by jumper J8/J10.

1.11 Hardware Installation

1. Set addressing, interrupts and output configuration jumpers on the card.
2. Turn unit off.
3. Remove system cover as instructed in the computer reference guide.
4. Insert card into a vacant slot following the guidelines for installation.
5. Replace system cover.

1.12 Software Installation

1.12.1 DOS Installation

This section briefly describes some of the files contained on the installation disk. Particularly:

- COMDRIVE.SYS
- QMODE.COM
- QCFG.EXE

The files on this disk are intended to be used with IOtech's multi-port ASYNC boards.

COMDRIVE.SYS

This program is installed with CONFIG.SYS and should be located at [C:\COMDRIVE.SYS]. COMDRIVE allows for the use of COM1 through COM34 as DOS devices. This means that 'COPY *.* COM5' (assuming that the board is there and it is configured) would work through DOS. COMDRIVE is written to be used with IOtech's multi-port async boards.

To install COMDRIVE.SYS add the following line to your CONFIG.SYS file:

```
device=C:\COMDRIVE.SYS
```

(or the actual location of the program COMDRIVE.SYS.)

QCFG.EXE

This program is used to maintain the COMDRIVE device driver.

The port addresses of COMDRIVE are configurable and need to be defined before any multi-port board will operate properly with QMODE.COM and DOS. After the multi port board is installed into the PC, COMDRIVE.SYS needs to be configured to recognize it. To do this the base address of the installed multi-port board(s) needs to be known.

Let's assume that the multi-port board has a base address of 300H (default), and let's also assume that it is a COM232/4PC QUAD PORT board. This would put port 1 of the board at a base address of 300H,port 2=308H, port 3=310H, and port 4=318H. Lastly, assume standard COM1 and COM2 boards are already installed in the PC.

To get COM3 up and running enter 'COM3=300' from the command line of QCFG. This will pipe data that goes from DOS COM3 to IOtech's multi-port board port 1. Then, to get COM4 activated, the command 'COM4=308' needs to be issued from QCFG, and so on for all other ports that are available.

QMODE.COM

This utility is used to configure COM1-COM34. It operates like the DOS MODE command. To use QMODE the syntax is:

```
QMODE COMn[:]baud[,[parity][,[length][,[stopbits]
```

where:

n of COMn is 1 - 34 for the proper async logical port

baud: 110,150,300,600,1200,2400,4800,or 9600 (only first 2 characters required, ie. "96")

parity: E(ven) (default), N(one), O(dd)

length: 7 (default), 8

stopbits: 1 (default), 2

Example: QMODE COM18:2400,n,8,1

This command will configure logical COM address 18 to be 2400 baud, no parity, 8 bit, 1 stop bit.

1.12.1.1 Installing the Files

1. Add COMDRIVE to the CONFIG.SYS file
   ```
   DEVICE=COMDRIVE.SYS
   ```
2. Reboot, to recognize COMDRIVE.SYS
3. Run QCFG.EXE configure COMDRIVE.
   ```
   COM3=300
   :
   ```
4. Make sure, while in QCFG.EXE, to SAVE your modified configuration
   ```
   SAVE
   Y (answer yes to both questions)
   Y
   ```

:

5. Add QMODE commands to your AUTOEXEC.BAT for power-up configuration of the new COM PORTS

   ```
   QMODE  COM3:96,e,7,1
   ```

6. Reboot.

7. Now all defined COM ports should be addressable.

   `'COPY *.* COM3'` will work properly

1.12.2 Windows Installation

To install the IOtech Windows 3.1 versions of the communications drivers, follow these steps:

1. Select `Run` from either File Manager or Program Manager. This is in the File Menu for either of these.

2. Type `a:\setup`. This works if your source diskette is inserted in drive A. Use the appropriate drive letter of the disk drive for your source diskette.

3. Setup will install the new device drivers and will modify the appropriate Windows system files. There is an additional application, Com Config, which is placed in the IOtech App group file.

4. Run the IOtech Com Config application. This will allow you to configure the device drivers for things such as the I/O address, IRQ, baud rate, handshaking, etc. This application incorporates context sensitive help.